CLAIMS:

1. A method of providing ordered data to a device over a bus with a weakly ordered interface, the bus providing a communication path for data and associated addresses, comprising:

writing items of data into sequentially ordered areas of a memory to form a sequence of items of data, the sequentially ordered areas of memory being identifiable by addresses, each item of data being placed in an area having an associated address;

transmitting the items of data and the associated addresses over the bus;

receiving the items of data and the associated addresses from the bus;

examining the associated address for each item of data received from the bus; and

placing each item of data received from the bus in one of multiple sequentially arranged areas of a storing buffer, each item being placed based on the associated address of each item, the placement of the items of data forming the sequence of items.

2. The method of providing ordered data to a device of claim 1 wherein the items of data comprise commands and parameters, each parameter pertaining to a command.

3. The method of providing ordered data to a device of claim 2 further comprising examining the items of data to determine whether the items of data are commands or parameters.

4. The method of providing ordered data to a device of claim 3 further comprising determining which parameters pertain to a command.

5. The method of providing ordered data to a device of claim 4 further comprising reading an item of data from the storing buffer.

6. The method of providing ordered data to a device of claim 5 wherein the storing buffer has at least one associated read availability status array comprised of a plurality of read availability indicators, each of the multiple sequentially arranged areas of the storing buffer having a corresponding read availability indicator.

7. The method of providing ordered data to a device of claim 6 further comprising setting the corresponding read availability indicator of the read availability status array to indicate data availability for reading when data is placed in the corresponding area of the storing buffer.

8. The method of providing ordered data to a device of claim 7 further comprising setting the corresponding read availability indicator of the read availability status array to indicate data unavailability for reading when data is read from the corresponding area of the storing buffer.

9. The method of providing ordered data to a device of claim 8 wherein storing buffer comprises a plurality of storage buffers, and each of the storage buffers has an associated read availability status array.

10. The method of providing ordered data to a device of claim 9 further comprising reading an item of data from all of the storage buffers and placing the read items of data in a storage memory if all of the read availability status arrays indicate data available for reading, and reading an item from one of the

storage buffers and providing the read item to a command interpreter, which performs the steps of examining the items of data and determining which parameters pertain to a command, if at least one but less than all of the read availability status arrays indicate data available for reading.

11. The method of claim 10 wherein each of the storage buffers has an associated direct read status array comprised of a plurality of direct read status indicators, each of the multiple sequentially arranged areas of the storage buffer having a corresponding direct read status indicator, and the method further comprises setting the corresponding direct read status indicator to indicate a direct read if an item is read from a corresponding area of the storage buffer when less than all of the read availability status arrays indicate data availability.

12. The method of claim 11 further comprising setting all of the direct read status indicators to indicate not a direct read if each of the direct read status arrays indicate a direct read.

13. The method of claim 12 wherein status of the read availability status arrays and the direct read status arrays is determined by examining the read availability status arrays and the direct read status arrays, and examination and setting of the read availability status arrays and the direct read status arrays is performed on an indicator by indicator basis.

14. A method of increasing effective bus bandwidth comprising:

defining a region of a memory as a write combining memory type, the region of the memory being comprised of addressable locations of processor memory, the addressable locations identifiable by an address;

writing items of data into the region in a sequential order of addressable locations, the items of data comprising encoded commands and parameters associated with the encoded commands, with the number of parameters associated with the command and the meaning of parameters in the sequential order indicated by the encoded commands;

providing the items of data and addresses of the items of data over a bus to a coprocessor; and

arranging the items of data in an order corresponding to the sequential order of addressable locations upon receipt of the items of data by the coprocessor.

15. The method of increasing effective bus bandwidth of claim 14 further comprising determining which items of data in the order corresponding to the sequential order of addressable locations are encoded commands and further determining which parameters are associated with each encoded command and the meaning of the parameters based on their position in the order of addressable locations.

16. A bus interface unit of a computer device, the bus interface unit coupled to a bus with a weakly ordered interface providing information comprised of data items and associated addresses, comprising:

a plurality of storage buffers each having a plurality of slots for storing data items;

a first router for routing data items received from the bus to one of the plurality of storage buffers based on a first part of the address associated with the data item;

a plurality of second routers for each of the storage buffers for routing data items routed to a one of the storage buffers to one of the slots in the one of the storage buffers based on a second part of the address associated with the data item.

17. The bus interface unit of claim 16 further comprising means for providing data items stored in the plurality of slots to a command interpreter for determining if any of the data items corresponds to a command.

18. The bus interface unit of claim 17 wherein the plurality of storage buffers include means for indicating whether each of the plurality of slots contains data items not provided to the command interpreter.

19. The bus interface unit of claim 18 further comprising means for providing data items from one slot of each of the plurality of storage buffers to a temporary storage area, and means for providing data items stored in the temporary storage area to the command interpreter.

20. The bus interface unit of claim 19 wherein the plurality of storage buffers include means for indicating whether each of the plurality of slots contained data provided to the command interpreter without the data being first provided to the temporary storage area.

21. The bus interface unit of claim 20 further comprising a receive FIFO, with the first router routing data items received from the bus to one of the plurality of storage buffers by way of the receive FIFO.

22. The bus interface unit of claim 21 wherein data is received by the bus interface unit at a bus clock rate and the bus interface unit operates at the computer device clock rate, and the receive FIFO is input data at the bus clock rate and outputs data at the computer device clock rate.

23. A computer device for reordering incoming data received from a bus interface, the incoming data having associated address information, comprising:

a receive buffer which receives the incoming data;

a storage buffer which stores the incoming data in an order based on the associated address information; and

a decoder which determines proper placement of the incoming data in the receive buffer in the storage buffer based on the associated address information.

24. The computer device of claim 23 wherein the storage buffer further comprises a tag array to indicate that data is stored in a portion within the buffers.

25. The computer device of claim 24 wherein the storage buffer further comprises hit arrays to indicate that data can not be stored in a specific portion within the storage buffer.

26. The computer device of claim 25 further comprising graphics memory connected to the storage buffer and able to store blocks of data retrieved from the storage buffer.

27. The computer device of claim 26 further comprising:

a central processor; and

a computer program executing on the central processor, wherein the computer program causing the central processor to send the incoming data over the bus interface.

28. The computer device of claim 27 wherein the receive buffer synchronizer is a FIFO.

29. The computer device of claim 28 wherein the storage buffer comprises a plurality of 32 bit DWords.

30. A method of reordering incoming data from a data source, the incoming data containing address information, the incoming data being in a predefined order in the data source and being transmitted from the data source in an order other than the predefined order, the method comprising:

receiving the incoming data transmitted from the data source;

arranging, in the predefined order, the incoming data based on the address information contained within the incoming data; and

storing the arranged data temporarily.

31. The method of claim 30 further comprising indicating that the arranged data is temporarily stored.

32. The method of claim 31 further comprising additionally storing the arranged data into a series of blocks of contiguous data.

33. The method of claim 32 further comprising processing the arranged data stored in the pre-defined order.

34. The method of claim 33 further comprising indicating that the arranged data that is temporarily stored is being processed.